M_2 Add + shift

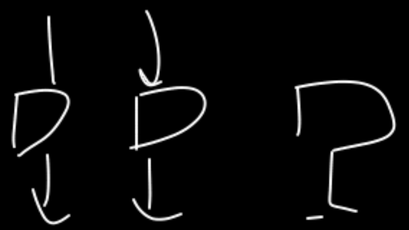
M_2 Add

↓ i

M_3

↓ Add

for i = 0 to 31 >



Addition

32 Add

32 Mult

Control unit

Registers | ALU

Caches

RAM

Circuits

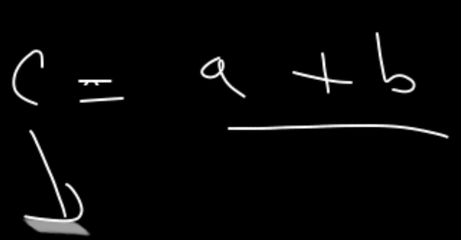
0 0 1 0 1 1 . 1

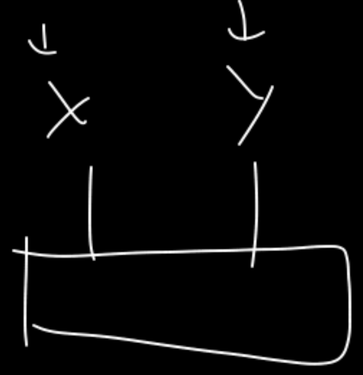
Processor

Registers - 32

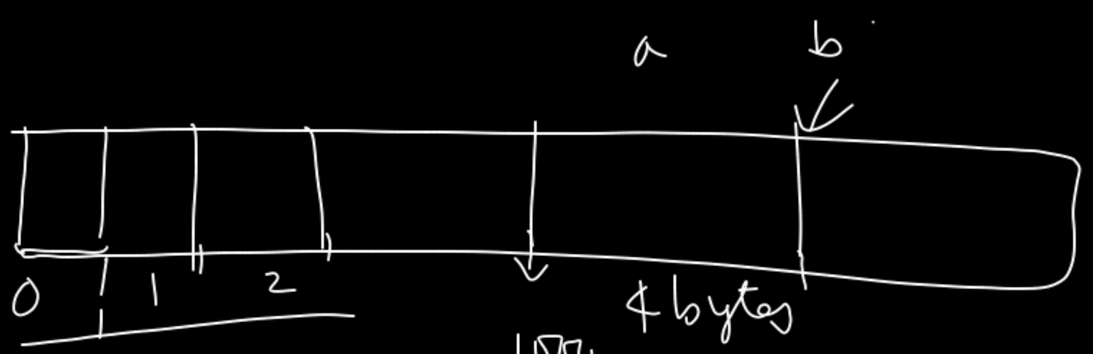
32 - Registers

$c = a + b$





int a;b;



&S2 = 1000

&S2 + 4

4 GB, byte = 8-bit

double q[5];

a + 16

8-bytes
40 bytes

s_7 s_3 s_4 s_5

d = a + b + c ;

```
add $t1, $s3, $s4
add $s7, $t1, $s5
```

$$f = (a+b) - (c+d)$$
$$s_1 \quad s_2 \; s_3 \quad s_4 \; s_5$$

add $t1, $s2, $s3
add $t2, $s4, $s5
sub $s1, $t1, $t2

$a = b + 10$
t

double A; ↘ ↓

int_ a = A[5] + b ;

A → $s1
b → $s2
a → $s3
$t0

lw $t0, 20($s1)